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SPACE VECTOR BASED TRANSISTOR-CLAMPED CASCADED MULTILEVEL INVERTER

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Abstract*—The inverter configurations with higher number of output voltage levels have the ability to modulate waveforms with a better harmonic spectrum. A Three phase cascaded multilevel inverter which uses five-level transistor clamped H-bridge power cells is presented. In this, Multi Carrier Phase Shifted Pulse Width Modulation technique is applied for the balanced power distribution among the power cells. This PWM technique is applied for both Sine PWM and Space Vector PWM. The output voltage harmonics and the motor current harmonics are observed and compared for both techniques. The proposed inverter is simulated under MATLAB/Simulink environment on an induction motor model. From the results, the proposed inverter provides higher output quality with less harmonic distortion as compared to the other conventional inverters.

Keywords*—Transistor clamped H-Bridge cell, Cascaded multilevel inverter, SVPWM, Multicarrier phase-shifted pulse width modulation.

I. INTRODUCTION

The technology of developing multilevel inverter has been growing because of the demand for high-voltage, high power converters. These are capable of producing high quality waveforms while utilizing low-voltage devices and reduced switching frequency with regards to semiconductor power switch voltage limits. The modified multilevel outputs are superior in quality in reducing filter requirement and overall system size. As the switching frequency is reduced, switching losses are also reduced and high-power quality is maintained.

The multilevel inverter implementation has done in different applications ranging from medium to high power levels such as renewable energy generation and distribution [1], [2], motor drives [3], [4], power conditioning devices [5]. There are three major conventional multilevel inverter topologies namely the diode-clamped or Neutral-point-clamped (NPC) inverter [6], flying capacitor multilevel inverter [7] and cascaded multilevel inverter [8]. Many other topologies like NPC have been introduced for various industrial applications [9], [10]. Different modulation techniques used for multilevel inverters are space vector modulation (SVM) [11], [12], carrier-based pulse-width modulation [13]-[15], staircase or fundamental frequency modulation [16] and selective harmonic elimination [17], [18].

Here the cascaded multilevel inverter is mainly focused because of its modularity in achieving best fault tolerance and control simplicity [19]. Usually by connecting several identical H-bridge cells in cascade at the output side, we can achieve and low harmonic distortion medium-voltage operation [20]. The important advantages of 'H' converters are the number of DC sources used is reduced to 50% which reduces the size and complexity, they can only produce an odd number of levels which ensure the existence of the '0-v' level at the load.

In this paper, symmetrical cascaded inverter possible of increase in voltage level without varying dc voltage with same number of power cells is proposed. Now-a-days, the transistor clamped converter topology has improved which has the advantage of requiring same number of power transistors as the number of levels generated and therefore the number of semiconductors is also reduced [21]. Instead of clamping the connection points between the capacitors and switches through diodes, it is done using bidirectional switches. This gives a controllable path for the clamping devices [22].

A cascaded multilevel inverter with two inverter with two inverter legs in series is proposed in [20] in which more cells are required and this tends to the increase in number of isolated dc sources as well as bulky transformers even though the number of switches for each cell required is lower. The proposed new configuration makes use of a five-level Transistor Clamped H-Bridge (TCHB) as a power cell which can produce a five-level output instead of three-level as with the conventional H-bridge [22], [23]. The proposed inverter is compared with the SVPWM technique applying to the multicarrier phase-shifted pulse width modulation on an Induction motor. Simulation results are presented to verify the validities of the proposed inverter.

II. PROPOSED CONVERTER TOPOLOGY

Fig. 1(a) shows the general configuration of the proposed inverter which comprises of N_c series-connected five-level TCHB cells. Fig. 1(b) is the proposed single-phase five-level PWM inverter cell. One switching element and four diodes which are combined known as bidirectional switch added in the conventional full-bridge inverter and is connected to the centre-tap of dc power supply. Proper switching control of the auxiliary switch can generate half level of dc supply voltage. The cell is able to produce five output voltage levels (0, ± (1/2) v_{dc}, ± v_{dc}) based on the switching combinations given in Table I. The number of power cells required mainly depends on the operating voltage and manufacturing cost. In this case, a two cell configuration can produce a high quality output which can generate up to 17-voltage levels.

In general, the relation for the maximum number of levels of the phase-to-neutral voltage v_{aN} (t) and the line-to-line output voltage v_{ab} (t) based on N_c cells are respectively represented by

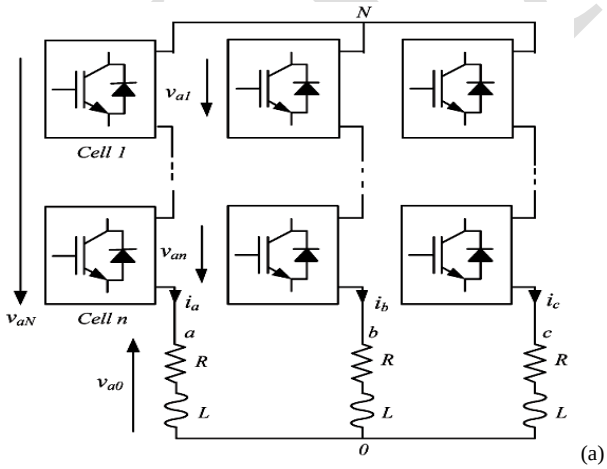
$$n_p = 4\,N_c + 1 \quad (1)$$

$$n_l = 8\,N_c + 1 \quad (2)$$

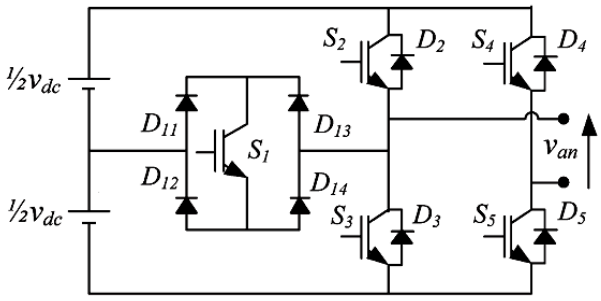
Based on the possible switch combinations, S_1-S_5 in Table I, the power cell output voltage v_{an} can be given by

$$v_{an} = v_{dc}\left(S_{5n} - S_{4n}\right)\left\{\frac{1}{2}S_{1n} + \left|S_{2n} - S_{4n}\right| \cdot \left|S_{3n} - S_{5n}\right|\right\} \quad (3)$$

From the summation of the power cell voltage, the phase-to-neutral voltage, v_{an} and line voltage, v_{ab} are denoted



(a)



(b)

Fig. 1. TCHB: (a) General configuration of the proposed three- phase cascaded multilevel inverter and (b) topology of five level transistor-clamped H-bridge for each cell.

TABLE I

FIVE-LEVEL TRANSISTOR CLAMPED H-BRIDGE OUTPUT VOLTAGE

S_1	S_2	S_3	S_4	S_5	v_{an}
0	1	0	0	1	v_{dc}
1	0	0	0	1	½ v_{dc}
0	0 or 1	1 or 0	0 or 1	1 or 0	0
1	0	0	1	0	-½ v_{dc}
0	0	1	1	0	-v_{dc}

respectively as

$$v_{an} = \sum_{n=1}^{N_c} v_{an} \quad (4)$$

$$v_{ab} = v_{an} - v_{bn} \quad (5)$$

III. MODULATION STRATEGY

PWM techniques have been developed for inverter circuits to reduce the magnitude of harmonics and to allow control of fundamental component of output voltage. In the proposed topology, Multicarrier Phase-shifted PWM (CPS-PWM) modulation is used to generate the PWM signals.

Basic principle of the proposed switching strategy is to generate gate signals by comparing the reference signal with the two carrier waves. The amplitude and frequency of all triangular carrier waves are the same as well as the phase shifts between adjacent carrier waves. For signal generation in each cell, one carrier signal and two voltage references are used [24]. Both reference waves are similar but displaced by an offset equal to the carrier's amplitude which is ½.

The reference signals v_{ref1} and v_{ref2} are derived from a full-wave voltage reference, v_{ref} defined by

$$v_{ref} = M \sin \omega t \quad (6)$$

$$v_{ref1} = |v_{ref}| \quad (7)$$

$$v_{ref2} = v_{ref1} - \frac{1}{2} \quad (8)$$

The modulation index M of the proposed method is defined by

$$M = \frac{1}{2}\frac{v_{ref}}{v_{cr}} \quad (9)$$

Depending on the number of cells, the phase shift in the carrier wave for each cell $\theta_{Cr,\,n}$ can be obtained from

$$\theta_{Cr,n} = \frac{2\pi(n-1)}{N_c},\ n = 1, 2\ldots N_c \quad (10)$$

When the voltage reference is between $0 < v_{ref} \leq (1/2)$, v_{ref1} is compared with the triangular carrier and when S_5 is in ON state, switches S_1 and S_3 operate alternately to produce either ½ v_{dc} or 0. Whereas, when the reference is during the interval $(1/2) < v_{ref} \leq 1$, v_{ref2} is compared and when S_5 is in ON state, switches S_1 and S_2 operate alternately to produce either ½ v_{dc} or v_{dc}. If the reference voltage is between $-(1/2) < v_{ref} \leq 0$, v_{ref1} is compared and when S_4 is ON, switches S_1 and S_2 alternately produce either -½ v_{dc} or 0. If the reference voltage is between $-1 < v_{ref} \leq -(1/2)$, v_{ref2} is compared with the carrier and when S_4 is ON, switches S_1 and S_3 alternately produce either -½ v_{dc} or v_{dc}. From this, we can notice that the two switches S_4 and S_5 only operate in each reference half cycle. This implies that

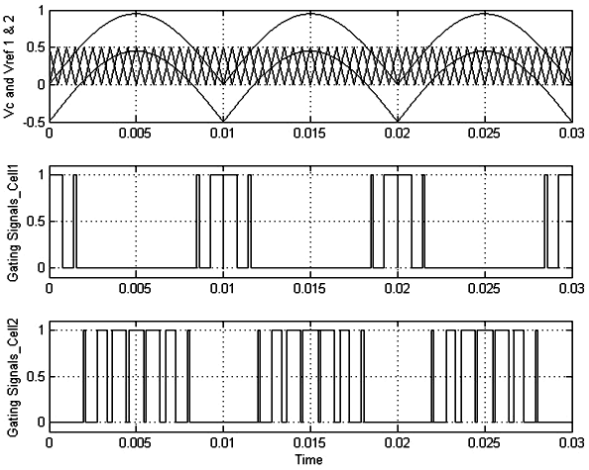


Fig. 2. Multicarrier phase-shifted PWM for two-cell configuration

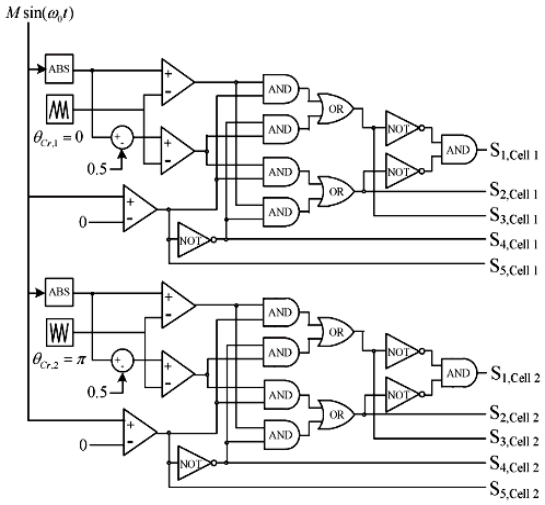


Fig. ***3. PWM signal generation with multicarrier phase-shifted modulation for phase a.***

both switches S_4 and S_5 operate at the fundamental frequency and the remaining switches operate close to the carrier frequency. Hence the dc voltage will be switched at low frequency and so the switching losses are reduced.

Fig. 2 shows the modulation scheme used for the proposed two-cell configuration and fig. 3 shows the block diagram for generating the PWM signals. The five-level output voltage will be generated from each cell. The phase-to-neutral voltage v_{aN} which is obtained based on the voltage reference magnitude and the combination of cell voltages v_{a1} and v_{a2} are listed in Table II.

From Table II, we can observe a total of nine levels ($\pm 2\ v_{dc}$, $\pm (3/2)\ v_{dc}$, $\pm v_{dc}$, $\pm (1/2)\ v_{dc}$, 0) phase-to-neutral voltages when both cells are cascaded with CPS-PWM modulation. The phase voltages are displaced by (2/3)π from each other and hence higher levels of line voltages will be produced for v_{ab} from (5).

TABLE II

PHASE-TO-NEUTRAL OUTPUT VOLTAGE FOR TWO-CELL CONFIGURATION

	v_{a1}	v_{a2}	v_{aN}
$0 < v_{ref} \leq ½$	0	0	0
	½ v_{dc}	0	½ v_{dc}
	0	½ v_{dc}	½ v_{dc}
	½ v_{dc}	½ v_{dc}	v_{dc}
$½ < v_{ref} \leq 1$	½ v_{dc}	½ v_{dc}	v_{dc}
	v_{dc}	½ v_{dc}	3/2 v_{dc}
	½ v_{dc}	v_{dc}	3/2 v_{dc}
	v_{dc}	v_{dc}	2 v_{dc}
$-½ < v_{ref} \leq 0$	0	0	0
	-½ v_{dc}	0	-½ v_{dc}
	0	-½ v_{dc}	-½ v_{dc}
	-½ v_{dc}	-½ v_{dc}	- v_{dc}
$-1 < v_{ref} \leq -½$	-½ v_{dc}	-½ v_{dc}	- v_{dc}

	- v_{dc}	-½ v_{dc}	-3/2 v_{dc}
	-½ v_{dc}	- v_{dc}	-3/2 v_{dc}
	- v_{dc}	- v_{dc}	-2 v_{dc}

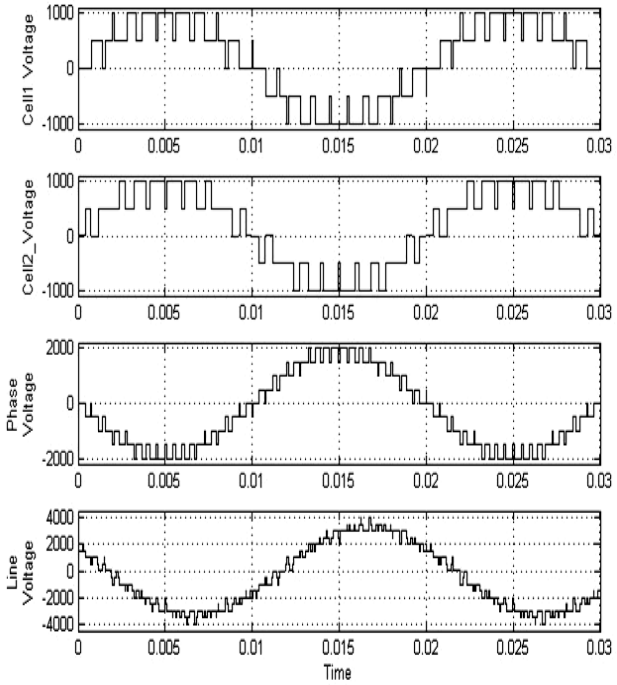
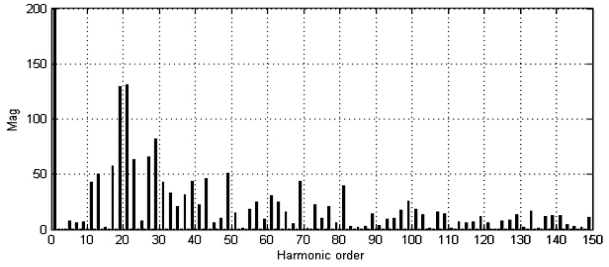


Fig. 4. Simulated output voltages of proposed inverter



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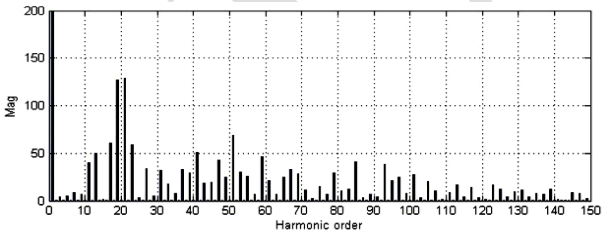

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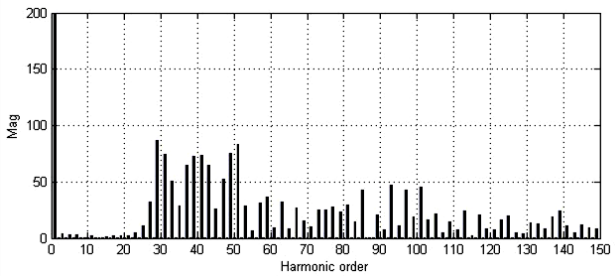

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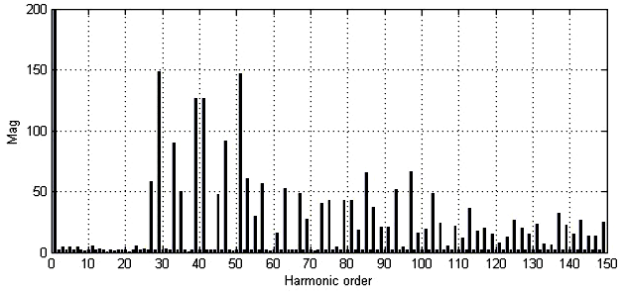


(d)

Fig. 5. Harmonic spectrum of the proposed inverter (a) Cell 1 output voltage harmonics (b) Cell 2 output voltage harmonics (c) Phase voltage harmonics (d) Line voltage harmonics

IV. RESULTS

4.1 R Load

Fig. 4 shows the output voltage for the two-cell configuration from the simulation results. The modulating signal's modulation index and frequency are 0.95 and 50 Hz respectively. The carrier waves have a maximum frequency of 1 kHz and there is 180^o phase-shift between each other. The supply given to each cell is 1 kV dc voltage. Each cell

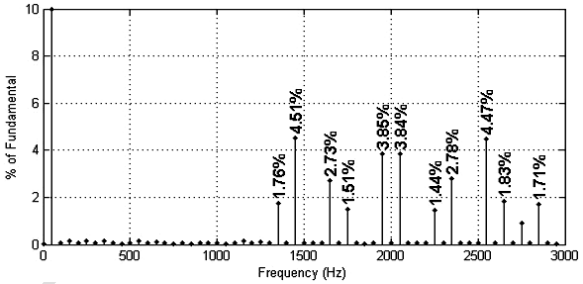


Fig. 6. Harmonic spectrum of line voltage

produces five-level voltage. In the phase voltage of the inverter, nine levels are produced and in the line voltage, 17 levels are produces which provides high output quality.

The harmonics and frequency components of the output voltages obtained from the FFT analysis using MATLAB are shown in Fig. 6. The harmonic spectrum of line voltage with respect to frequency measured up to 998th harmonic is shown in Fig. 7 with THD of 30.16% and the fundamental RMS voltage of 148.5 V.

4.2 Induction Motor

The proposed transistor clamped multilevel inverter is fed to a three-phase Induction motor. The voltage supplied to each cell is 220 V dc and the carrier frequency is 1 kHz. Fig. 7 shows the nine-level phase-to-neutral output voltage of the model. The three phase current, torque and speed of the Induction motor at transient and steady state are shown in Fig. 8. The harmonics of the current is also presented in Fig. 9 and noted as 5.35% with a fundamental RMS value of 3.667 A.

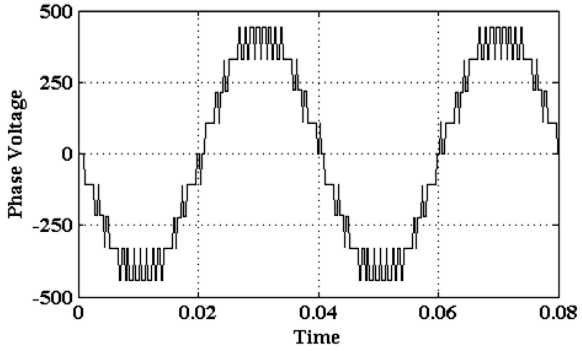
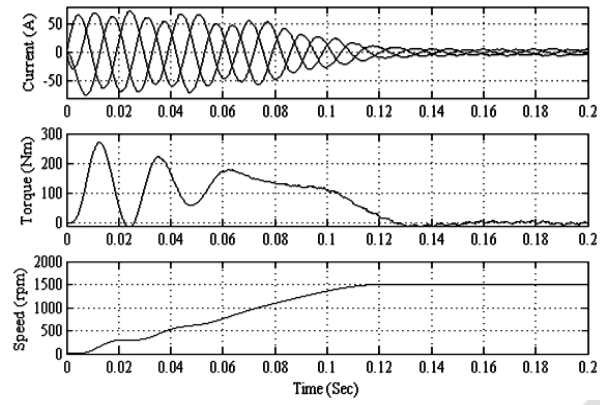


Fig. 7. Nine-level phase-to-neutral output voltage



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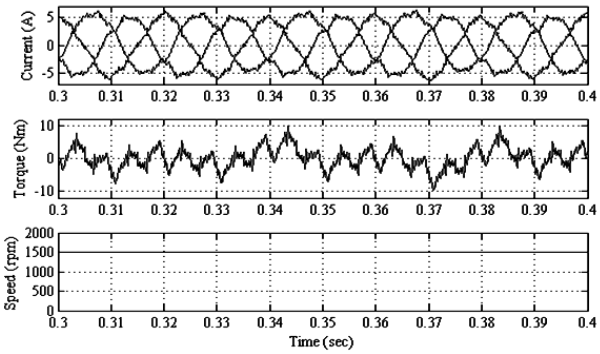


(b)

Fig. 8. (a) Simulation waveforms of Current, Torque and Speed of Induction motor with SPWM (b) at Steady state

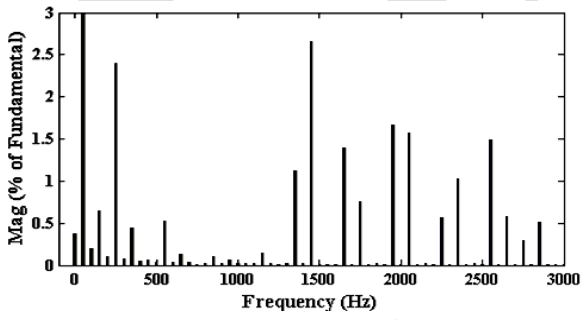


Fig. 9. Harmonics of current

V. SVPWM BASED PROPOSED TOPOLOGY

SVPWM technique generates sine wave that provides a higher voltage to the motor with lower total harmonic distortion. Important advantage of SVPWM is the minimization of the current ripple and/or the total losses of the power converter. The SVPWM technique is analyzed based on the effective time. Effective time is the time duration when the voltage difference is not zero which happens because an effective power flow is made during this duration. When the switching states of each phase goes to 0 from 1 during one sampling interval at different times, an effective voltage is introduced and the time duration for that is denoted as T_{eff}

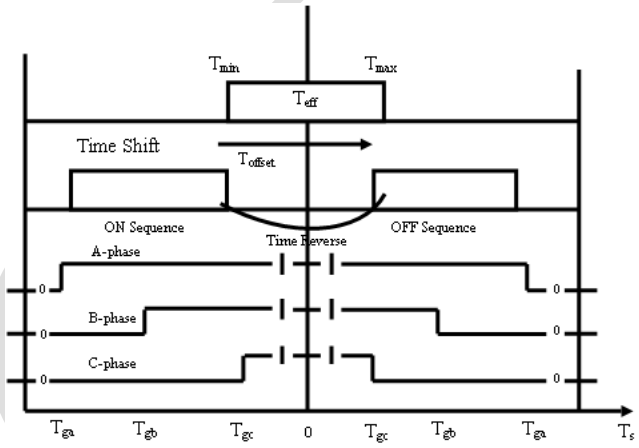


Fig. 10. Actual gating time generation

which is known as 'Effective time'. T_s denotes the sampling time.

An imaginary time value is introduced which is directly proportional to the phase voltage and the relation is as follows.

$$V_{as}^* : V_{dc} = T_{as} : T_s \Rightarrow T_{as} = \frac{T_s}{V_{dc}} \cdot V_{as}^*$$

$$V_{bs}^* : V_{dc} = T_{bs} : T_s \Rightarrow T_{bs} = \frac{T_s}{V_{dc}} \cdot V_{bs}^*$$

$$V_{cs}^* : V_{dc} = T_{cs} : T_s \Rightarrow T_{cs} = \frac{T_s}{V_{dc}} \cdot V_{cs}^* \qquad (11)$$

V_{as}^*, V_{bs}^* and V_{cs}^* are the A-phase, B-phase and C-phase reference voltages respectively. The imaginary time is called the "Imaginary switching time".

The time duration between the largest and smallest of three imaginary times is called the effective time and is given by

$$T_{eff} = T_{\max} - T_{\min} \qquad (12)$$

Where T_{min}= min (T_{as}, T_{bs}, T_{cs}), T_{max}= max (T_{as}, T_{bs}, T_{cs})
To generate the actual getting times (T_{ga}, T_{gb}, T_{gc}), a time shifting operation will be applied to the imaginary switching times which is done by adding the offset time as shown in Fig. 10.

$$T_{ga} = T_{as} + T_{offset}$$
$$T_{gb} = T_{bs} + T_{offset} \quad (13)$$
$$T_{gc} = T_{cs} + T_{offset}$$

To generate the symmetrical switching time within two sampling intervals, the actual switching time should be replaced by the subtraction value with sampling time as follows.

$$T_{ga} = T_s - T_{ga}$$
$$T_{gb} = T_s - T_{gb} \quad (14)$$
$$T_{gc} = T_s - T_{gc}$$

For the full utilization of DC link voltage, the gating times should be limited to a value between 0 and T_s as follows.

$$0 \le T_{\min} + T_{offset},\ T_{\max} + T_{offset} \le T_s$$

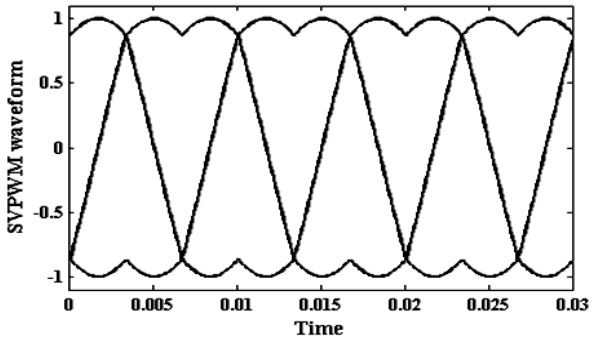


Fig. 11. Modulating waveform of SVPWM

In SVPWM method, according to the reference vector location, the applying times should be combined with the zero voltage applying time T_0 which is distributed symmetrically at the start and end of the sampling interval in a symmetrical manner. Hence, to reposition the effective time at the center of the sampling interval, the time-shifting value T_{offset} is

$$T_{offset} = \frac{1}{2}T_0 - T_{\min}$$

where

$$T_0 = T_s - T_{eff} \quad (15)$$

Fig. 11 shows the modulating waveform obtained from SVPWM. Now the SVPWM waveform is applied instead of sine wave in the multicarrier phase-shifted pulse width modulation technique and the pulses generated are applied to the transistor clamped multilevel inverter fed Induction motor. Fig. 12 shows the nine-level phase-to-neutral output voltage. Fig. 13 shows the waveforms of Current, Torque and Speed at transient and steady state.

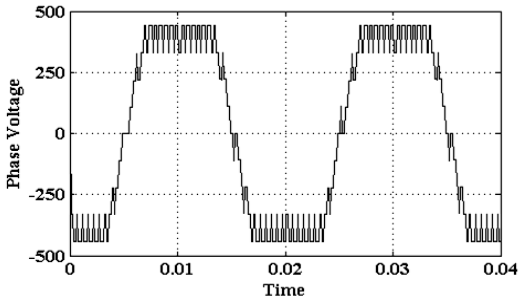
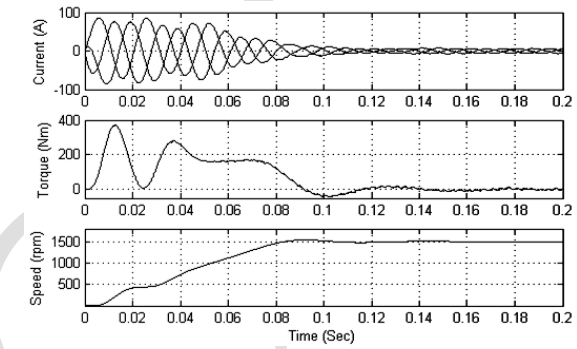


Fig. 12. Nine-level phase-to-neutral output voltage with SVPWM



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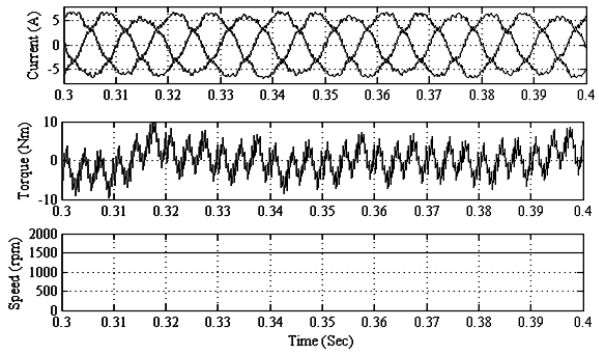

(b)

Fig. 13. (a) Simulation waveforms of Current, Torque and Speed of Induction motor with SVPWM (b) at Steady state

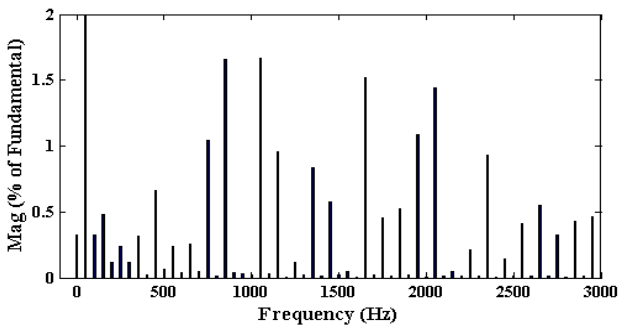

Fig. 14. Harmonics of current

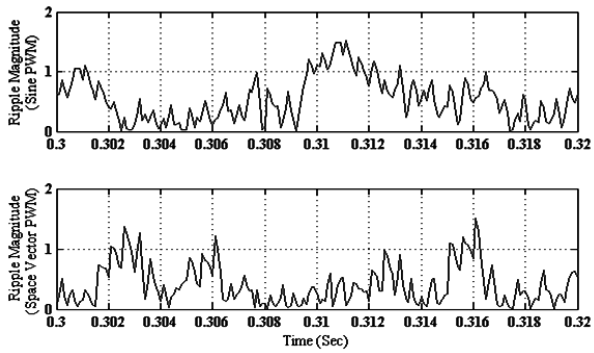

Fig. 15. Ripple currents of SPWM and SVPWM

The harmonics of the current is represented in Fig. 14 and noted as 4.32% with a fundamental RMS value of 4.459 A. The ripple currents of SPWM and SVPWM are shown in Fig. 15. The ripple current magnitude is less for SVPWM compared to SPWM above 0.5.

VI. CONCLUSION

In this paper, a Transistor clamped cascaded multilevel inverter with multicarrier phase-shifted pulse width modulation using SPWM and SVPWM is presented. The output voltages along with harmonics were presented with R load and the outputs of current, torque and speed of induction motor load were presented for both SPWM and SVPWM. Here, SVPWM has more advantages such as reduction of THD and low ripple current.

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